Nanomachining of mesoscopic electronic devices using an atomic force microscope

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(Received 28 April 1999; accepted for publication 25 June 1999)

An atomic force microscope (AFM) is used to locally deplete the two-dimensional electron gas (2DEG) of a GaAs/AlGaAs heterostructure. The depletion is induced by repeated mechanical scribing of the surface layers of the heterostructure using the AFM tip. Measuring the room-temperature resistance across the scribed lines during fabrication provides *in situ* control of the depletion of the 2DEG. Variation of the room-temperature resistance of such lines tunes their low-temperature characteristics from tunneling up to insulating behavior. Using this technique, an in-plane-gate transistor and a single-electron transistor were fabricated. © *1999 American Institute of Physics.* [S0003-6951(99)00234-X]

Atomic force microscopes (AFMs) are powerful tools for the creation of sub-micron structures.[1] Among others, one promising way of using the AFM as a lithographic tool is the mechanical scratching of surfaces with the AFM tip. Hereby, the normal force between the moving tip and the surface is raised above a threshold leading to the formation of a groove in the surface. So far, this method was used to structure various materials like metals,[2] polymer films,[3] combined polymer metal resists[4] and even relatively hard semiconductor surfaces.[5] An interesting field for the application of AFM based lithography is its use on GaAs/AlGaAs heterostructures. The two-dimensional electron gases (2DEGs) realized in these systems are used as a model for the examination of low-dimensional electronics.[6] So far, some work was done on local anodic oxidation of 2DEGs[7] and on indirect mechanical machining via polymer resists.[8] Recently, direct patterning of a 2DEG was demonstrated on the relatively soft InAs/AlSb system by fabricating antidot arrays.[9] In this letter, we present a new approach to a well-defined machining process on the relatively hard GaAs cap layer of a GaAs/AlGaAs heterostructure: we *in situ* measure the resistance across the written barriers and therefore the impact of the lithographical process on the electronic properties of the underlying 2DEG. Using this method, mesoscopic electronic devices like an in-plane-gate transistor (IPG) and a single-electron transistor (SET) were fabricated.

For our experiments, we used heterostructures grown by molecular beam epitaxy consisting from top to bottom of a 5 nm GaAs cap layer, 40 nm of Si-doped AlGaAs, a 10 nm undoped AlGaAs barrier, a 20 nm GaAs quantum well containing the 2DEG and a 30 nm undoped AlGaAs barrier grown on a GaAs buffer layer. 20 μm wide standard Hall bars were defined by photolithography and wet chemical etching. They show a low temperature electron density of 6.1×10^{15} m^{-2} and electron mobilities of 10.9 m^2/Vs.

First, we consider the fabrication of individual lines written into the 2DEG. In the inset of Fig. 1(a), the experimental setup of the AFM writing process is sketched. For simplicity, only two ohmic contacts of the Hall bar are shown. The samples are bonded and electrically contacted inside the AFM allowing to *in situ* measure the resistance R of the 2DEG across the written line at room temperature. During the writing process, the AFM detection laser is switched off and the sample is kept in the dark to avoid that the resistance of the 2DEG is masked by a low-ohmic parallel conducting channel through the illuminated GaAs wafer. The writing process is carried out moving the AFM cantilever against the surface resulting in contact forces in the range of 50 μN when using standard AFM tips.[10] Applying such high contact forces the tip is repeatedly scanned over the Hall bar with a scan velocity of about 100 μm/s leading to a stepwise depletion of the 2DEG underneath the tip and thus an increase of R.

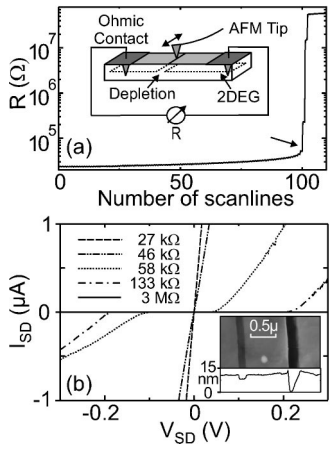

FIG. 1. (a) Room-temperature resistance R during the scratching of a line against the number of scans with a high force of 50 μN. The tip is scratched back and forth over the Hall bar leading to a local depletion of the 2DEG (inset). (b) Current–voltage curves at 4.2 K across mechanically fabricated lines. R varies between 27 kΩ and 3 MΩ. Above $R\approx50$ kΩ strong nonlinearities occur due to the local depopulation of the 2DEG. Inset: two lines fabricated by 20 (left) and 120 (right) scans with a force of 50 μN.

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Figure 1(a) shows the resistance R of the 2DEG during the fabrication of a typical line. It is plotted against the number of scans with an applied high contact force of 50 μN. During the repeated writing, the value of R continously increases from its starting value of $R \approx 20$ kΩ defined by the intrinsic resistance of the 2DEG at room temperature and the contact resistances. First, R grows slowly. After 75 scans the resistance across the structure has increased by 6 kΩ. Subsequently, R rises faster and after about 100 scan lines R rapidly grows from $R \approx 50$ kΩ up to $R \approx 55$ MΩ (see arrow). Upon further increase of the number of scans, R remains basically unchanged. We ascribe this behavior of R to a step-by-step depletion of the 2DEG due to a continous removal of the surface layers of the GaAs/AlGaAs heterostructure. First, the undoped GaAs cap layer of the heterostructure is removed resulting in a weak depletion of the 2DEG due to a relocation of electrons from the 2DEG into newly created surface states of the written groove. Then, the doping layer is continously thinned down leading to a stronger depopulation of the 2DEG in the vicinity of the line. At the AlGaAs surface, the Fermi energy is pinned in the middle of the band gap. Removing the surface layers of a 2DEG brings the pinned Fermi level closer to the 2DEG. As a consequence, the conduction band in the GaAs quantum well is effectivly lifted and therefore locally depleted. In this respect, our technique is similar to a shallow etch process[11] where the surface layers of a heterostructure are removed chemically causing the depletion of the 2DEG. The more of the surface is removed the higher the conduction band is lifted and, as a consequence, the stronger the local depopulation of the 2DEG. Eventually, the 2DEG is completely depopulated and the background resistance of the wafer of about 55 MΩ is measured.

The inset in Fig. 1(b) shows an AFM micrograph of two lines fabricated this way (upper panel) and a cross section through both lines (lower panel). The lines were written applying the same force of about 50 μN. For the left line, the fabrication was stopped after 20 scans resulting in a depth of 4 nm and a width of about 140 nm. The writing of the right line was stopped after 120 scans when the 2DEG was completely depopulated. The measured depth of the line of 12 nm shows that roughly 7 nm of the 40 nm thick donor layer are removed. For our samples with the 2DEG situated 55–75 nm below the surface, the minimum lateral feature size of such high-resistance grooves was found to be smaller than 100 nm. A further reduction of the linewidth should be possible using different heterostructures with the 2DEG located closer to the surface thus facilitating the depopulation of the 2DEG.

In Fig. 1(b), the current measured across such lines at a temperature of 4.2 K is depicted. The source-drain current I_{SD} is plotted as a function of the applied bias voltage V_{SD}. The writing of the lines was stopped at different predefined values of R between $R = 27$ kΩ and 3 MΩ. The shape of the I–V curves depends strongly on R. The low-resistance curves ($R = 27$ and 46 kΩ) show a linear current voltage dependence around zero bias. This indicates a weak depletion of the 2DEG underneath the line leaving its metallic character untouched. The next two I–V curves belonging to lines with higher values of $R = 58$ and 133 kΩ are strongly nonlinear.

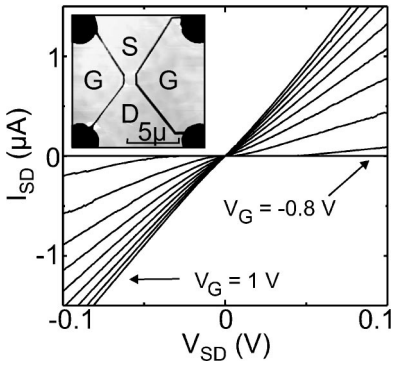

FIG. 2. Mechanically fabricated IPG with source S, drain D, and side-gates G (inset). I–V curves taken at 4.2 K between source and drain at side-gate voltages V_G in the range of $V_G = 1, \ldots, -0.8$V, $\Delta V_G = 0.2$ V. The characteristics change from ohmic transport ($V_G = 1$ V) to insulating behavior ($V_G = -0.8$ V).

Here, the current is suppressed at low source-drain voltages V_{SD}. This behavior can be explained in terms of the creation of tunneling barrieres under the scribed grooves in the GaAs surface. The 2DEG is locally depleted giving rise to an energetic barrier for the electrons in the quantum well. Around zero bias, the barrier inhibits transport whereas the application of a source-drain voltage leads to a bending and therefore an effective lowering of the barrier causing the current onset at a certain threshold voltage. A similar behavior was also observed across barriers written by local anodic oxidation on an AlGaAs heterostructure.[7] Generally spoken, tunneling characteristics in the I–V curves at liquid helium temperatures were found in our samples when R exceeded ≈ 50 kΩ. For $R \lesssim 50$ kΩ, linear characteristics are measured. The $R = 3$ MΩ line shows total insulation in the displayed region. Here, the current sets in at about $V_{SD} \approx 4$ V (not shown). When the machining was stopped at $R \gtrsim 10$ MΩ, the barriers created were insulating up to $V_{SD} > 50$ V. Since their low-temperature resistance exceeds 50 GΩ, they are ideal candidates for the fabrication of in-plane gates as shown in Fig. 2.

The inset in Fig. 2 shows an AFM micrograph of an in-plane-gate transistor (IPG)[12] with mechanically written gates. Source S and drain D are connected by a 1.2 μm wide conducting channel separated from the side-gates G by 110 nm wide insulating grooves. Figure 2 shows I–V curves between source and drain of such an IPG taken at 4.2 K at various side-gate voltages V_G. At $V_G = 1$ V, a linear behavior is observed. With lower side-gate voltages nonlinearities around zero bias occur and at $V_G = -0.8$ V, the current is completely suppressed in the displayed region, i.e., the transistor is switched off. Variation of V_G between $V_G = -0.8$ and 1 V changes the conductance of the channel by more than four orders of magnitude proving effective transistor operation.

Using such an IPG, a SET can be fabricated writing two tunneling barriers across the conducting channel. In Fig. 3(a), an AFM micrograph of such a SET is presented. The addition of two tunneling barriers (1) to the IPG channel creates a side-gated SET island (2). Figures 3(b)–3(c) show transport measurements of such a device at 350 mK. In Fig. 3(b), an I–V curve between source and drain at a side-gate voltage $V_G = 0.186$ V is shown. A zero bias suppression of the current due to Coulomb blockade and adjacent steps in

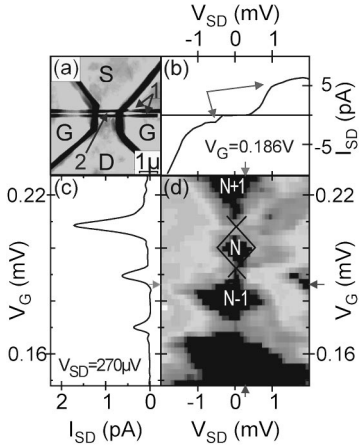

FIG. 3. (a) Mechanically fabricated SET with two tunneling barriers (1) forming an island (2) between source *S*, drain *D*, and side-gates *G*. (b)–(d): SET characteristics at $T=350$ mK. (b) Source-drain current I_{SD} against bias voltage V_{SD} at fixed gate voltage $V_G=0.186$ V. A step-like behavior is observed (arrows). (c) Coulomb-blockade oscillations at constant bias $V_{SD}=270$ μV. I_{SD} (x axis) is plotted against V_G (y axis). (d) Gray-scale plot of the differential conductance G_{SD} under variation of bias V_{SD} and side-gate voltage V_G. Black color: $G_{SD}<10^{-10}$ S; white color: $G_{SD}>10^{-8}$ S. Diamond-shaped Coulomb-blockade regions (dark) with constant electron number ($N_e=N, N\pm1$) on the island appear.

the current in virtue of single-electron tunneling (see arrows) are observed. Varying the side-gate voltage V_G the potential of the island can be tuned. In Fig. 3(c), the source-drain current I_{SD} (x axis) is plotted as a function of the side-gate voltage V_G (y axis) at a constant bias $V_{SD}=270$ μV. Clear Coulomb-blockade oscillations are observed. Peaks in I_{SD} marking single-electron tunneling and regions of vanishing current due to Coulomb blockade[6] occur. From the periodicity $\Delta V_G=0.02$ V of the Coulomb-blockade oscillations, a gate capacitance of $C_G=8$ aF can be calculated. The transition between Coulomb blockade and single-electron tunneling can be seen more completely in Fig. 3(d). Here, a gray scale plot of the differential conductance $G_{SD}=\partial I_{SD}/\partial V_{SD}$ calculated from I–V curves at different side-gate voltages V_G is displayed. Around zero bias the typical diamond-shaped regions of vanishing conductance appear (see, e.g., guiding lines around N). The transport is suppressed due to Coulomb blockade and the number of electrons on the SET island, N_e, is constant ($N_e=N, N\pm1, \ldots$). Changes of V_G lead to a shift of the energy levels of the electrons on the island and therefore a variation of the width of the Coulomb blockade in V_{SD}. In the transition between states with neighboring electron number ($\Delta N_e=1$), Coulomb blockade is lifted and single-electron transport is allowed. From the maximal width of the Coulomb gap at $N_e=N-1$, a total capacitance of the island of $C_{\text{tot}}=1.1\times10^{-16}$ F can be deduced. Assuming a simple model of a disk-shaped dot, an island diameter of about 250 nm can be estimated which is comparable to the geometrical size defined by mechanical fabrication.

In conclusion, direct AFM nanomachining of the surface layers of GaAs/AlGaAs heterostructures provides a powerful tool to fabricate tunneling barriers as well as insulating gates in a 2DEG. During the fabrication the resistance of the 2DEG can be *in situ* controlled providing a good measure of the local depletion of the 2DEG and therefore of the characteristics of the fabricated barrier. An in-plane-gate transistor and a single-electron transistor working at low temperatures were fabricated demonstrating the feasibility of direct AFM nanomachining for the fabrication of future electronic devices.

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