ELSEVIER

Physica E 6 (2000) 860–863

PHYSICA E

www.elsevier.nl/locate/physe

Controlled mechanical AFM machining of two-dimensional electron systems: fabrication of a single-electron transistor

H.W. Schumacher[a,*], U.F. Keyser[a], U. Zeitler[a], R.J. Haug[a], K. Eberl[b]

[a] *Institut für Festkörperphysik, Universität Hannover, Appelstraße 2, 30167 Hannover, Germany*
[b] *Max-Planck-Institut für Festkörperforschung, Heisenbergstr. 1, 70569 Stuttgart, Germany*

Abstract

By mechanical scratching the surface of a GaAs/AlGaAs heterostructure with an atomic force microscope an energetic barrier for the two-dimensional electron gas is formed. The barrier formation is in situ controlled by measuring the room-temperature resistance across the barrier. Barrier heights can be tuned from some mV up to more than 100 mV as determined by measurement of the thermally activated current. Low-resistance barriers show typical tunnelling behaviour at low temperatures whereas high-resistance lines show GΩ resistances in a bias range up to some 10 V allowing their use as in-plane gates. Transport measurements of a side gated single-electron transistor fabricated this way are presented. © 2000 Elsevier Science B.V. All rights reserved.

PACS: 07.79.Lh; 85.40.Hp; 73.23.Hk; 73.23.b; 73.61.Ey

Keywords: AFM; Nanofabrication; Single-electron tunnelling; Heterostructures

One way of using the atomic force microscope (AFM) as a lithographic tool is the mechanical scratching of surfaces with the AFM tip (see as a review, e.g. Ref. [1]). The increase of the contact force between tip and surface above a certain threshold leads to the formation of a groove in the surface. Various materials from polymers to metals and semiconductors were patterned this way [2–5]. Using this method on an InAs surface quantum well opens a possibility to the direct AFM fabrication of mesoscopic electronic structures as demonstrated by Cortes Rosa et al. [6]. The depletion of the two-dimensional electron gas (2DEG) of a standard GaAs/AlGaAs heterostructure was demonstrated by local anodic oxidation of the GaAs surface [7,8]. Here, we show how mechanical scratching of the surface of a GaAs/AlGaAs heterostructure can be used for the local depletion of the 2DEG situated about 55 nm below the surface. This way electronic barriers for the 2D electrons can be formed.

Our heterostructures were grown by molecular beam epitaxy and they consist from top to bottom of a 5 nm GaAs cap layer, 40 nm of Si-doped

---

[*] Corresponding author. Tel.: +49-511-762-2523; fax: +49-511-762-2904.

E-mail address: schumach@nano.uni-hannover.de (H.W. Schumacher)

PII: S1386-9477(99)00230-1

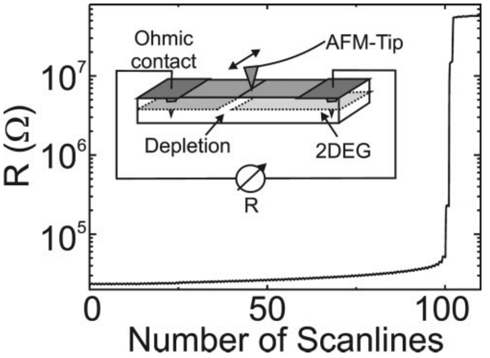

Fig. 1. 2DEG resistance R during fabrication against the number of scans with increased force. Inset: Sketch of the controlled mechanical AFM machining.

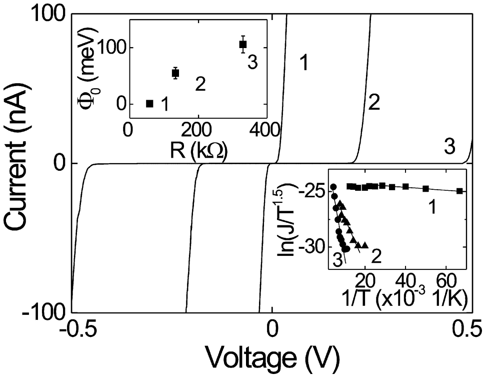

Fig. 2. *IV* curves of barriers (1)–(3) taken at 1.5 K: (lower inset) 2D Arrhenius plot of the same barriers; (upper inset) barrier heights Φ_0 plotted against room temperature resistance R.

AlGaAs, a 10 nm undoped AlGaAs barrier, a 20 nm GaAs quantum well containing the 2DEG and a 30 nm undoped AlGaAs barrier grown on a GaAs buffer layer. 20 μm wide standard Hall bars were defined by photolithography and wet chemical etching showing a low-temperature electron density of 6.1×10^{15} m^{-2} and electron mobilities of 10.9 m^2/V s.

The influence of scribing the surface on the resistance of the sample is displayed in Fig. 1 with the principle of operation of the controlled mechanical AFM machining depicted in the inset. An electrically contacted Hall bar is mounted in the AFM. The machining process is performed pressing the tip[1] nominally some μm against the surface while multiply scanning along a line over the Hall structure. Contact forces are around 50 to 100 μN with a scan velocity of 100 μm/s. During fabrication the room temperature resistance R of the 2DEG across the written line is controlled. The AFM laser is switched off and the sample is kept in the dark to reduce photoconductivity of the bulk material. In Fig. 1 the measured resistance R of a barrier is plotted against the number of scanlines with a force of 50 μN. The resistance slowly rises from its starting value of around 20 kΩ. After 75 scans R rises faster and after about 100 scan lines R rapidly grows from 50 kΩ up to 55 MΩ, the background resistance of the GaAs, whereafter only minor changes occur. This raise of R can be ascribed to a local depletion of the 2DEG due to a local removal of the surface layers of the heterostructure comparable to a shallow etch process [9]. Due to the in situ control of the 2DEG resistance the fabrication of the barriers can be stopped at any predefined value of R opening the possibility of fabricating barriers with tunable characteristics. High resistance grooves ($R \sim$ MΩ) show lateral sizes from around 400 down to less than 100 nm and depths up to 25 nm as measured by AFM and scanning electron microscopy. Lower resistance lines in general show smaller lateral dimensions and lower depths.

In the following the behaviour of three barriers named (1)–(3) having room temperature resistances of $R = 58$, 133, and 330 kΩ, respectively, will be discussed. At room temperature their current–voltage dependencies do not show strong nonlinearities. In Fig. 2 current–voltage characteristics of the three barriers taken at 1.5 K are displayed. All devices show a suppressed current around zero bias as expected for a tunneling barrier in the 2DEG. With increasing R the onset of the current shifts towards higher bias voltages caused by a rising height of the tunnelling barrier. Barrier heights Φ_0 above the Fermi energy E_F can be deduced from thermal activation measurements [10]. Activated currents I were measured at bias voltages between 0.5 and 200 mV in a temperature range from $T = 1.5$–200 K in a continuous He flow cryostat. In a 2D system the saturation current density J obeys the 2D Richardson law,

$$J = AT^{1.5}\exp\left(\frac{-\Phi_0}{k_B T}\right), \tag{1}$$

---

[1] Non-contact Si AFM tips, Nanosensors.

where $A = e\sqrt{m^*}k_B^{1.5}/\hbar^2(2\pi)^{1.5}$ is the 2D Richardson constant with e, m^* the electron's charge and effective mass [11]. Therefore, Arrhenius plots of the form $\ln(I/T^{1.5})$ versus $1/T$ allow the deduction of the barrier heights Φ_0 from the gradient of the plots. Such a plot is shown in the lower inset of Fig. 2 for the three barriers under discussion. The bias voltages of the displayed data are 1 mV for barrier 1 and 150 mV for barriers 2 and 3. The straight lines mark the gradients used for the determination of Φ_0 at these bias voltages. Values of Φ_0 are calculated from gradients at various bias voltages. Errors are calculated from the standard deviation of these values. The such derived barrier heights are 1 ± 0.4 meV (1), 55 ± 10 meV (2), and 106 ± 16 meV (3). The upper inset of Fig. 2 shows Φ_0 as a function of room temperature resistance R. As can be seen from the plot Φ_0 raises almost linearly with increasing R. In other words measurement of R during the mechanical fabrication provides good control of the height of the barrier in fabrication.

At temperatures of a few Kelvin the *IV* characteristics of barriers having a room temperature resistance in the MΩ range show a suppressed current up to bias voltages of some 10 V (not displayed). The corresponding barrier heights Φ_0 thus by far exceed the 100 meV measured e.g. for device (3). Their leakage resistances greater than 50 GΩ make these high-resistance lines ideal candidates for the fabrication of in-plane gates [12]. Mechanical AFM machining therefore provides means of directly writing in-plane gates [13] as well as tunnelling barriers which opens the possibility of fabricating a single-electron transistor (SET) (see as a review e.g. Ref. [14]).

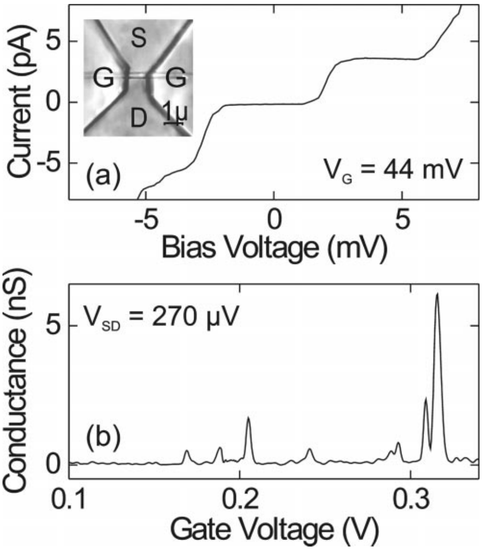

Fig. 3. Mechanically fabricated SET. $T = 350$ mK: (a) Coulomb blockade staircase in the *IV* characteristics. Inset: AFM micrograph of a mechanically fabricated SET; (b) Coulomb blockade oscillations under variation of gate voltage.

A such fabricated SET is shown in the inset of Fig. 3(a). Source S and drain D are separated from the gates G by high-resistance lines forming a conducting channel of about 1 μm width. Two tunnelling barriers are added to the channel defining a SET island in the 2DEG. In Fig. 3(a) current–voltage characteristics taken at 350 mK of such a device are presented. Clear steps caused by Coulomb blockade are observed. A total capacitance of 110 aF is deduced from the width of the Coulomb blockade. Assuming a simple model of a disk-shaped dot a diameter of 250 nm can be calculated which is comparable to the geometrical dimension of the device. Fig. 3(b) shows the conductance between source and drain at a fixed bias as a function of gate voltage. Peaks in the conductance assigned to single-electron tunnelling are separated by regions of suppressed transport due to Coulomb blockade. The energy levels of the SET can be effectively shifted applying a voltage to the side gates.

In conclusion mechanical AFM machining was used to create grooves in the surface layers of a GaAs/AlGaAs heterostructure. Using this technique tunnelling barriers with variable heights from 1 to more than 100 meV were fabricated in the 2DEG. The room temperature resistance R of the 2DEG across the written grooves was found to be a good measure for the barrier height Φ_0. Therefore measurement of R provides in situ control of the barrier formation process. Additionally to the fabrication of tunnelling barriers in-plane gates can be written into the 2DEG by stopping the machining process at higher values of R ($R \sim$ MΩ). A side-gated single-electron transistor was fabricated proving the feasibility of mechanical AFM machining for the fabrication of mesoscopic electronic devices.

References

[1] C.R.K. Marrian (Ed.), Proc. IEEE 85 (1997) 481.

[2] X. Jin, W.N. Unertl, Appl. Phys. Lett. 61 (1992) 657.

[3] T. Sumomogi, T. Endo, K. Kuwahara, R. Kaneko, T. Miyamoto, J. Vac. Sci. Technol. B 12 (1994) 1876.

[4] B. Irmer, R. H. Blick, F. Simmel, W. Gödel, H. Lorenz, J. P. Kotthaus, Appl. Phys. Lett. 73 (1998) 2051.

[5] R. Magno, B.R. Bennett, Appl. Phys. Lett. 70 (1997) 1855.

[6] J. Cortes Rosa, M. Wendel, H. Lorenz, J.P. Kotthaus, M. Thomas, H. Kroemer, Appl. Phys. Lett. 73 (1998) 2684.

[7] M. Ishii, K. Matsumoto, Jpn. J. Appl. Phys. 34 (1995) 1329.

[8] R. Held, T. Vancura, T. Heinzel, K. Ensslin, M. Holland, W. Wegscheider, Appl. Phys. Lett. 73 (1998) 262.

[9] H. van Houten, B.J. van Wees, M.G.J. Heijman, J.P. André, Appl. Phys. Lett 49 (1986) 1781.

[10] M. Rossmanith, K. Syassen, E. Böckenhoff, K. Ploog, K. von Klitzing, Phys. Rev. B 44 (1991) 3168.

[11] A.J. Peck, S.J. Bending, K. von Klitzing, K. Ploog, Appl. Phys. Lett 62 (1993) 1544.

[12] A.D. Wieck, K. Ploog, Appl. Phys. Lett 56 (1990) 928.

[13] H.W. Schumacher, U.F. Keyser, U. Zeitler, R. J. Haug, K. Eberl, Appl. Phys. Lett. 75 (1999) in press.

[14] U. Meirav, E.B. Foxman, Semicond. Sci. Technol. 10 (1995) 255.