Fabrication of a single-electron transistor by current-controlled local oxidation of a two-dimensional electron system

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(Received 4 August 1999; accepted for publication 24 November 1999)

The surface layers of a GaAs/AlGaAs heterostructure are locally oxidized using an atomic force microscope. The local anodic oxidation depletes the underlying two-dimensional electron gas leading to the formation of tunneling barriers. The height of the barriers is determined by measuring the thermally activated current. By varying the oxidation current, the barrier heights can be tuned between a few meV and more than 100 meV. Using these barriers as tunneling elements, a side gated single-electron transistor is fabricated. © *2000 American Institute of Physics.* [S0003-6951(00)02304-4]

Local anodic oxidation (LAO)[1] using an atomic force microscope (AFM) is an effective way to modify the electronic properties of semiconductor[2] as well as metal[3] surfaces on the nanometer scale.[4] Various devices from a quantum-point contact[5] to a single-electron transistor[6] were fabricated this way. An interesting field of application of LAO is its use on GaAs/AlGaAs heterostructures.[7] Here the modification of the surface layers of the heterostructure induces a local depletion of the underlying two-dimensional electron gas (2DEG) giving rise to the formation of an electronic barrier in the 2DEG. The use of such fabricated oxide lines for the insulation of gate electrodes was demonstrated by the fabrication of a side-gated quantum-point contact.[8] In this letter we explore the possibility of fabricating defined tunneling barriers in a 2DEG by means of LAO applying a controlled current. The feasibility of this technique is demonstrated by the fabrication of a single-electron transistor (SET).

Figure 1 sketches the setup of our LAO experiments. The heterostructure consists of a 5 nm thick GaAs cap layer grown on 5 nm undoped AlGaAs, 15 nm of Si doped AlGaAs, a 15 nm thick undoped AlGaAs barrier and 500 nm of GaAs. The 2DEG lies 40 nm underneath the surface and has an electron density of 4×10^{15} m^{-1} and a low-temperature mobility of 23 m^2/V s. 10 μm wide Hall bars were defined using standard optical lithography and contacted with annealed AuGe/Ni pads. Hall bars were bonded on a chipcarrier and mounted into the AFM such that the samples could be contacted electrically. The AFM was utilized in contact mode using commercially available highly doped Si cantilevers.[9] Anodic oxidation of the sample surface was performed in ambient conditions applying constant currents I_{ox} from 50 nA up to 1 μA between the negatively biased tip and one of the Hall contacts.[10] During oxidation the applied bias was measured to obtain the tip–sample resistance. The best results were obtained using tips with tip–sample resistances in the MΩ range resulting in oxidation voltages of a few V. Higher tip–sample resistances require higher biases for similar currents, which increases the possibility of electrical discharges from the tip destroying the device. Additionally the tip wear is increased due to higher electrostatical forces between tip and sample.[11] The standard writing speed was 250 nm/s. In the lower right of Fig. 1, a typical oxide line fabricated by a current of 100 nA is displayed. The evenly shaped line is 50 nm wide and about 2 nm high due to the volume expansion of the oxide. The typical linewidths were between 30 nm ($I_{ox}=50$ nA) and 200 nm ($I_{ox}=1\,\mu$A).

In the following the influence of the LAO current on the electronic properties of the 2DEG will be discussed. As an example the low-temperature characteristics of three lines (*A*, *B*, and *C*) written across the Hall bar using the same tip with currents of 100, 400, and 700 nA, respectively, are compared. Figure 2 shows current–voltage ($I-V$) characteristics across the three devices taken at 1.3 K. In contrast to $I-V$ curves of an unstructured Hall bar, strong nonlinearities around zero bias occur. The low bias suppression of the cur-

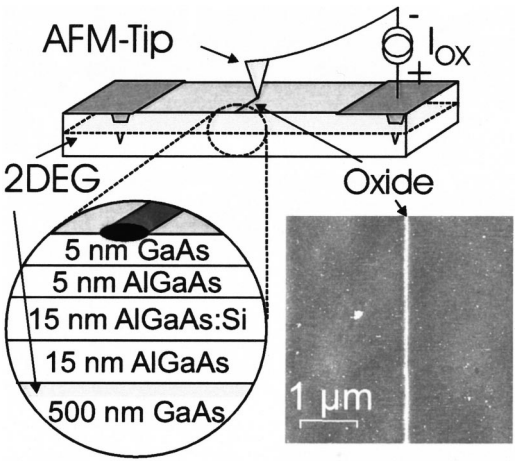

FIG. 1. Sketch of the local anodic oxidation setup: A constant current is applied between the negatively biased tip and one of the contacts of the Hall bar. (Lower right) Oxide line fabricated applying a current of $I_{ox}=100$ nA.

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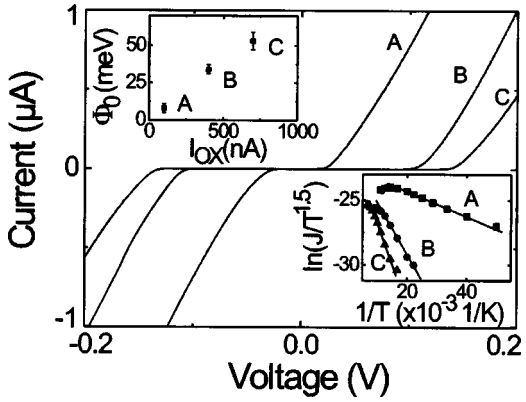

FIG. 2. Characterization of tunneling barriers fabricated by oxidation currents of 100 (*A*), 400 (*B*), and 700 nA (*C*). Current–voltage curves taken at 1.3 K. (Lower inset) 2D Arrhenius plot of the activated current at 2 mV bias. (Upper inset) Barrier heights Φ_0 vs oxidation currents I_{ox}.

rent speaks for the formation of tunneling barriers in the 2DEG underneath the oxide lines. Higher oxidation currents shift the current onset in the $I-V$ curves toward higher bias voltages. This can be attributed to the formation of higher tunneling barriers with an increasing value of I_{ox}. The barrier heights were determined measuring the thermally activated current across the barriers.[12] The experiments were done using a He flow cryostat at temperatures T between 1.3 and 140 K in a bias range between 1 and 50 mV. In two-dimensional (2D) systems the saturation current density J across a barrier with a height Φ_0 above the Fermi level obeys the Richardson law

$$J = AT^{1.5} \exp\left(\frac{-\Phi_0}{k_B T}\right), \tag{1}$$

where $A = e\sqrt{m^*}k_B^{1.5}/\hbar^2(2\pi)^{1.5}$ is the 2D Richardson constant with e, m^* the electron's charge and effective mass.[13] Therefore, Φ_0 can be deduced from the gradient of a $\ln(I/T^{1.5})$ vs $1/T$ Arrhenius plot, where $I = wJ$ is the activated current across the barrier in a channel with width w. The lower inset of Fig. 2 shows such a plot for the three devices under discussion. The applied bias is 2 mV. In contrast to the results reported by Held *et al.*[8] a linear dependence of the activated current in the 2D Arrhenius plot is found providing clear evidence for 2D tunneling behavior. Thus, the deduction of the barrier heights Φ_0 from the gradients is feasible. Linear fits used for the determination of Φ_0 are plotted as straight lines. Values of Φ_0 of 8 ± 2 (*A*), 34 ± 4 (*B*), and 53 ± 8 meV (*C*) are obtained. Φ_0 is displayed as a function of I_{ox} in the upper inset of Fig. 2. Φ_0 behaves almost linearly with I_{ox} making the oxidation current a good measure for the controlled fabrication of tunneling barriers. Although the LAO process is inherently tip dependent, similar results were obtained from experiments with different tips. This points to a good applicability of the current-controlled local oxidation for the fabrication of nanostructure devices. Low-temperature $I-V$ characteristics of barriers written with high values of I_{ox} of 1 μA show wider low-bias suppressions of the current up to bias voltages of about 0.5 V (not shown). The corresponding barrier heights Φ_0 thus exceed the 50 meV measured for device (*C*) and can be estimated to be larger than 100 meV.

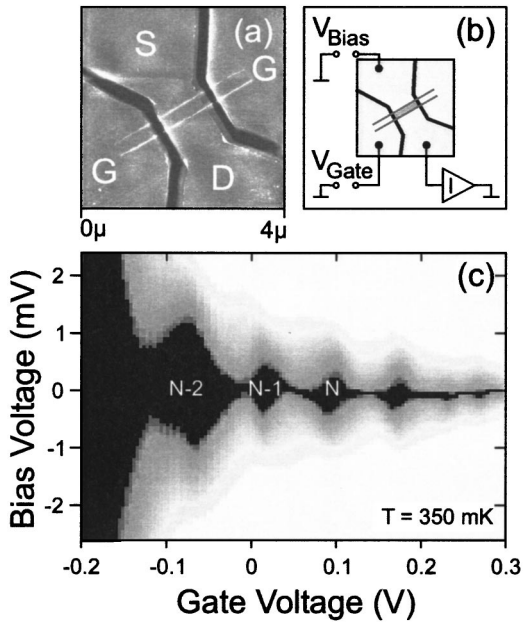

FIG. 3. AFM fabricated single-electron transistor with oxide tunneling barriers. (a) AFM micrograph: between source (*S*) and drain (*D*) an island is defined by two oxide lines (light lines). Mechanically machined gates (*G*) are located at the sides of the island (dark lines). (b) Measurement setup: $I-V$ curves are taken between source and drain applying various gate voltages at one of the side gates. (c) Coulomb-blockade diamonds at 350 mK: absolute value of the source–drain current $|I_{SD}|$ as a function of bias and gate voltage, (black: $|I_{SD}| < 0.5$ pA; white: $|I_{SD}| > 100$ pA). In the transition from $N-2$ to $N-1$ the conductance reaches a peak value of 150 nS (at $V_{Bias} = 340$ μV), whereas in the Coulomb-blockade regime values below 1 nS occur.

An explanation for the barrier formation was given by Held *et al.*[8] in terms of the so-called shallow etch process.[14] At the interface between the GaAs and its native oxide (i.e., the GaAs surface) the Fermi level is pinned near the center of the band gap. Removal of the surface layers of the heterojunction lifts the conduction band edge of the 2DEG as the pinned Fermi level is moved closer toward the GaAs/AlGaAs quantum well. Deeper etching leads to higher barriers as shown by experiments and numerical simulations of the conduction band profile under an etched trench.[13] A similar process is expected for oxidation of the heterostructure surface: the semiconductor–oxide interface is moved closer toward the 2DEG, thus forming a barrier in the 2DEG. On Si it was observed that higher oxidation currents increase the depths of the oxide formed.[15] From this we conclude that also on GaAs the oxide interface moves deeper into the bulk of the heterostructure with increasing current. Higher values of I_{ox} lead to the formation of higher barriers and hence, the observed $\Phi_0(I_{ox})$ dependence.

Using these locally oxidized barriers as tunneling elements, a side gated single-electron transistor[16] is fabricated. Figure 3(a) shows an AFM micrograph of such a device. In-plane gates (*G*) are fabricated by mechanical AFM machining (dark lines).[17] The channel between source (*S*) and drain (*D*) has a geometric width of 900 nm. Due to edge depletion in the vicinity of the gate lines the electronic width is expected to be in the range of 500 nm. Two tunneling barriers (light lines) are added to the channel by LAO ($I_{ox} = 150$ nA) shaping a 240 nm wide conducting island weakly coupled to the leads. The transport experiments were carried

out at $T=350$ mK. Current–voltage curves between source and drain were taken at gate voltages between -0.2 and 0.3 V. The gate voltage was applied to one of the side gates [see Fig. 3(b)]. In Fig. 3(c) a gray-scale plot of the absolute value of the source–drain current $|I_{SD}|$ is displayed as a function of gate (x axis) and bias voltage (y axis).

On the left side of the plot a dark region of vanishing current (i.e., vanishing conductance) is found over the whole displayed bias range. Transport across the island is inhibited and the SET is pinched off. Increase of the gate voltage brings about dark diamond-shaped regions of vanishing conductance around zero bias. Here, transport through the SET island is suppressed due to Coulomb blockade.[16] Energetically, the highest filled dot level is situated below the Fermi energy of source and drain, whereas the lowest empty level of the island lies well above the Fermi energies of the leads. Transport through the dot is not allowed and the electron number on the island remains constant ($n_e=N-2,N-1,N,\ldots$.) Application of a finite bias changes the Fermi levels (and therefore the chemical potentials) of the leads with respect to each other. At a certain bias an energy level of the dot is situated between the chemical potentials of the leads admitting transport (gray regions around the diamonds). The height (in the bias direction) of the Coulomb-blockade diamonds can be used to measure the Coulomb gap ΔE_C between two adjacent electron levels. From the maximum Coulomb gap at $n_e=N-2$, $\Delta E_C^{N-2}=1$ meV a total dot capacitance of $C_{\text{tot}}=160$ aF is deduced. Changes of the gate voltage shift the dot levels with respect to the chemical potentials of the leads. In the transition between two Coulomb-blockade diamonds (e.g., $N-2\rightarrow N-1$) the dot level now lies inbetween the chemical potentials of source and drain and single-electron tunneling occurs. The distance between the regions of single-electron tunneling as a function of gate voltage is defined by the total capacitance C_{tot} and the capacitive coupling between dot and gate. The periodicity and therefore the gate capacitance C_{Gate} can be obtained from a so-called Coulomb-blockade oscillation plot (I_{SD} vs V_{Gate} at low bias; not shown). The mean periodicity of $\Delta V_{\text{Gate}}=73$ mV corresponds to a gate capacitance of $C_{\text{Gate}}=2.2$ aF. In a simple model of an ungated 2D disk shaped dot the total capacitance C_{tot} is given by $C_{\text{tot}}=4\epsilon_0\epsilon_r D$, where D is the dot diameter, and $\epsilon_r=12.5$ is the dielectric constant of GaAs. From $C_{\text{tot}}=160$ aF we derive an island diameter of $D=360$ nm which is comparable to the geometric dimension of the dot (240 nm$\times$500 nm). Taking into account the major simplification of the model a good agreement between the geometric and electronic dimensions of the device is obtained.

In conclusion, we have studied the fabrication of tunneling barriers in a GaAs/AlGaAs heterojunction by means of local anodic oxidation of the heterojunction's surface. The oxidation was carried out by applying constant oxidation currents I_{ox} between the tip of an AFM and the sample. The energetic height of the barriers Φ_0 was determined via thermally activated transport measurements. Clear evidence for 2D tunneling behavior was found. Barrier heights between one and more than a hundred meV were derived. When using the same tip a linear relationship between I_{ox} and Φ_0 was seen, which allows us to tailor barriers with predefined values of Φ_0. Using such barriers as tunneling elements a single-electron transistor was fabricated, proving the feasibility of the current-controlled local oxidation for the fabrication of mesoscopic electronic devices.

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